IN THE SPECIFICATION

Please amend the paragraph beginning at page 4, line 5 as follows:

The present invention provides a solution to thickness, weight, and/or rigidity limitations in an electronic package, and to loop inductance problems that are associated with prior art electronic packages. FIG. 3 shows an electronic package 30 of the present invention that overcomes the inductive path problem yet still has sufficient mechanical integrity. The package 30 includes a die 32 mounted onto an interposer 34. The die 32 may be any type of IC, such as a processor, memory chip or chipset component. In an example embodiment, die 32 is mounted to the interposer 34 using a conventional C4 joint that is supplemented by an underfill. ~~Pins~~ Components 36 are mounted to the underside of the interposer 34. ~~Pins~~ Components 36 are positioned underneath the die 32 to electrically connect other electronic components, such as capacitors or I/O devices, to the underside of interposer 34 opposite to die 32. The ~~pins~~ components 36 can be mounted to the underside of interposer 34 using conventional surface mount technology. Thin interposer 34 reduces the distance between die 32 and any electronic components that are functionally connected to die 32 in order to minimize the inductive loop within package 30.